For the traces in this portion,
use intermal layers
and cover with Frame Ground plane.

RJ45

TX

CN1

TX+

TX-

R1 75

R2 75

R3 75

VJQ855055113

RX

CN2

RX+

RX-

R4 75

R5 75

R6 75

R7 75

R8 75

VJQ855055113

Transformer

TR1

VTSTLA6T118LF

C2 0.1u

C3 0.1u

R9 49.9

R10 49.9

R11 49.9

R12 49.9

Tie the connector shells
to Frame Ground.

2000V
C1
1000P

FG

VCK42R73D102K-1

Void +3.3V and Ground planes
underneath the transformer.

Tie to Frame Ground.

Connect to an input port of CPU.

LINK

LINK LED
(Green)

K A
LED
LN1371GTR

R15 330

R14 10k

PHY address is
set to 00000b
with internal
pull-down.

BCM5221(Broadcom)

PHY

IC1

VQCBCM5221KPTG

U:with pull_up 50k
D:with pull_down 50k

C9 10u

C10 0.1u

C7 0.1u

C11 0.1u

C8 0.1u

35	U_LNKLED#//TDI
36	U_SPDLED#/TMS
64	D_JTAG_EN
6	XTALI
5	XTALO
4	D_REF_CLK
31	TD+
30	TD-
26	RD+
25	RD-
14	D_PHYAD4
13	D_PHYAD3/PAUSE
12	D_PHYAD2/ACT_LED#
11	D_PHYAD1/COL_LED#
10	D_PHYAD0/FDX_LED#
21	D_SD+
19	D_SD-
39	D_FDX
37	U_F100/TCK
38	U_ANEN/TRST#
15	D_TESTEN
18	U_MII_EN
16	D_LOW_PWR
33	U_RCVLED#/TDO
60	D_TXD3
59	D_TXD2
58	D_TXD1
57	D_TXD0
53	TXC
56	D_TXEN
52	D_TXER
43	RXD3
44	RXD2
47	RXD1
48	RXD0
50	RXC
49	RXDV
51	RXER
61	COL
62	CRS
41	U_MDIO
42	D_MDC
17	EMERGY_DET
34	XMTLED#/INTR#
9	U_RESET#

R19 33

R20 33

R21 1.5K

R18 10K

C15 1000P

R17 100

34	TXD3(O)
35	TXD2(O)
36	TXD1(O)
37	TXD0(O)
43	TXC(I)
38	TXEN(O)
50	RXD3(I)
49	RXD2(I)
48	RXD1(I)
47	RXD0(I)
45	RXC(I)
42	RXDV(I)
41	RXER(I)
55	MDIO(I/O)
52	MDC(O)
82	U_TRST(I)
77	U_TCK(I)
84	U_TMS(I)
83	U_TDI(I)
94	TDO(O)
57	IVPD(I)
59	D_T_MODE1(I)
58	D_T_MODE0(I)
60	D_T_BUSMODE(I)
64	IXTAL(I)
62	OXTAL(I/O)
89	T_XRST(I)

Setting for
Master
16bits-bus

	MODE1	MODE0	BUSMODE
Master 16bits	0	0	0
Master 32bits	0	0	1
slave 16bits	0	1	0
slave 8bits	0	1	1

When 32bit-bus, tie pin 60 to +3.3V.
32bit-bus is more recomended
than 16bit-bus shown in this schematic.

R22 100

C20 1000P

RESET

Connect to an output port of CPU or system reset.
If a watchdog timer for the CPU overflows,
the RESET of PHY and MNM1221 should be set to LOW
for safety.

According to required EMC condition,
adjust CR filter close to RESET input of PHY and MNM1221.

C4 0.1u

X1

OE VDD

GND OUT

25MHz

R13 33

C5 0.1u

C6 10u

C12 0.01u

C13 0.1u

C14 10u

R16 1.24K ±1%

C16 0.1u

C21 0.1u

C17 0.1u

C22 0.1u

C18 0.1u

C23 0.1u

C19 0.1u

Place capacitors close to the following pairs.
pin3-4,15-16,28-29,39-40,53-54,78-79,89-90

ASIC

IC2

VQCMNM1221

U_:with pull-up 50k

D_:with pull-down 50k

T_:5V Tolerant

3	VDD0
28	VDD1
53	VDD2
78	VDD3
16	ADVDD0
33	ADVDD1
40	ADVDD2
66	ADVDD3
79	ADVDD4
89	ADVDD5
	ADVDD6
4	VSS0
15	VSS1
29	VSS2
40	VSS3
54	VSS4
65	VSS5
79	VSS6
90	VSS7
44	ADVSS0
51	ADVSS1
63	ADVSS2
91	ADVSS3

32	T_D31(I/O)
31	T_D30(I/O)
30	T_D29(I/O)
27	T_D28(I/O)
26	T_D27(I/O)
25	T_D26(I/O)
24	T_D25(I/O)
23	T_D24(I/O)
22	T_D23(I/O)
21	T_D22(I/O)
20	T_D21(I/O)
19	T_D20(I/O)
18	T_D19(I/O)
17	T_D18(I/O)
14	T_D17(I/O)
13	T_D16(I/O)
12	T_D15(I/O)
11	T_D14(I/O)
10	T_D13(I/O)
9	T_D12(I/O)
8	T_D11(I/O)
7	T_D10(I/O)
6	T_D09(I/O)
5	T_D08(I/O)
2	T_D07(I/O)
1	T_D06(I/O)
100	T_D05(I/O)
99	T_D04(I/O)
98	T_D03(I/O)
97	T_D02(I/O)
96	T_D01(I/O)
95	T_D00(I/O)

RNW1 10k

RNW2 10k

In Master,normally use 32bits-bus.

Data Bus

Address Bus
(unit: byte)

D[15-0]

A[16-1]

76	T_A10(I)
75	T_A09(I)
74	T_A08(I)
73	T_A07(I)
72	T_A06(I)
71	T_A05(I)
70	T_A04(I)
69	T_A03(I)
68	T_A02(I)
67	T_A01(I)
66	T_A00(I)

85	T_XCS(I)	CS
86	T_XWR(I)	WR
87	T_XRD(I)	RD
91	XLED/XWAIT(O)	WAIT
88	T_XTXIM(I)	TXTIM
93	XSYNC(O)	SYNC
92	XINTRX(O)	INTRX

Bus Control
Signals

Timing
Signals

PHY Configurations:

- Auto-Negotiation Disable
- 100BASE-TX
- Full-Duplex
- Auto-MDIX Disable
- PHY Address: 00h
- MII Mode

Rev. 2

PK100	PRINT CIRCUIT BOARD	581DTAKA1	@RELAT	1	KO	8
REF No.	PARTS NAME	CODE NO.	Relation	QTY	UNIT	TYPE

Scale	Designed	Drawn	Checked	Approved	Sheet
	FUJISAKI		.	.	
	2011/01/14		.	.	

Model: MNM1221

Name: Reference Circuit (BCM5221)

No.: SR-MNM1221-BCM

SVD_E