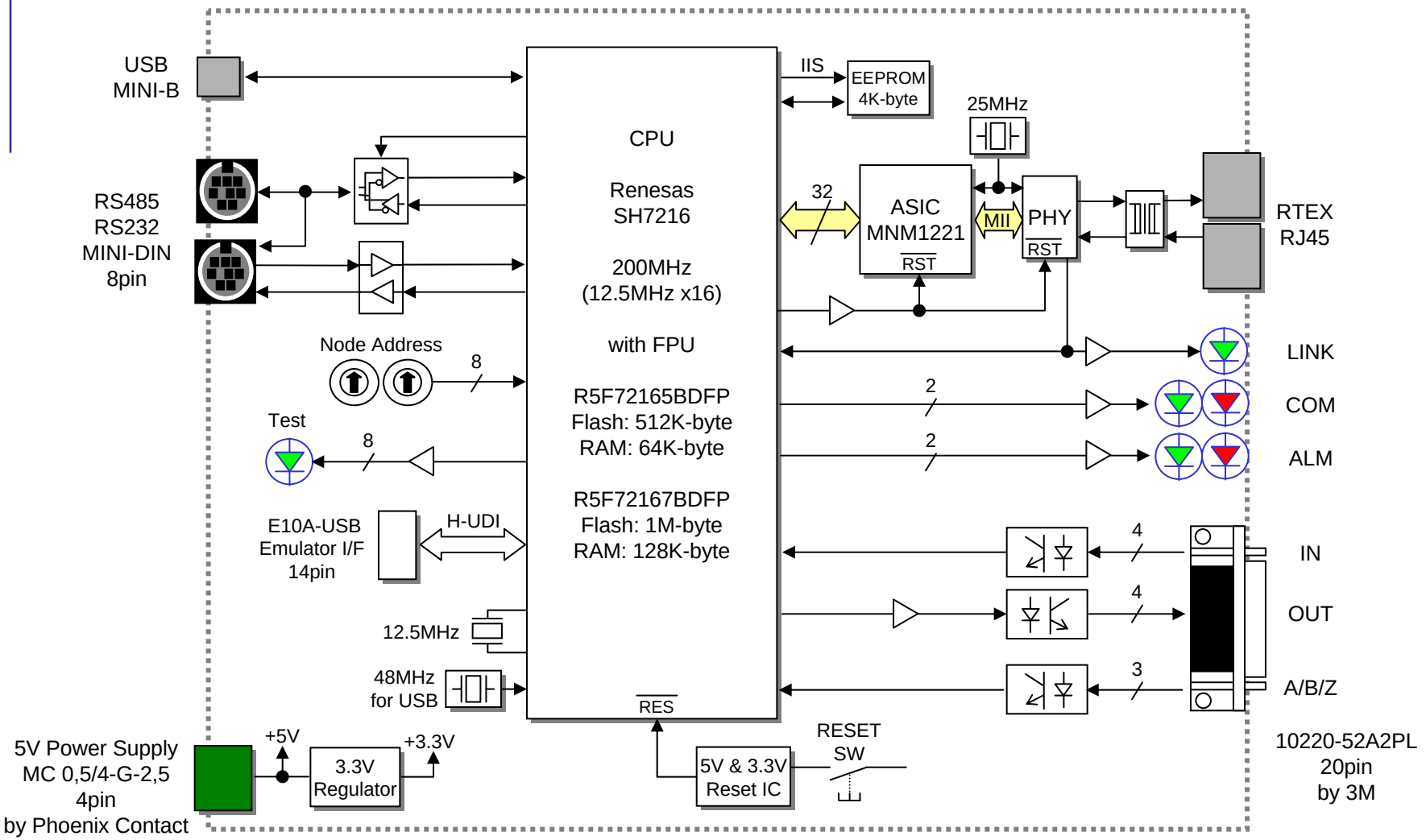
RTEX module “581D744”
Hardware Description

Motor Business Unit
Appliances Company

Revision History

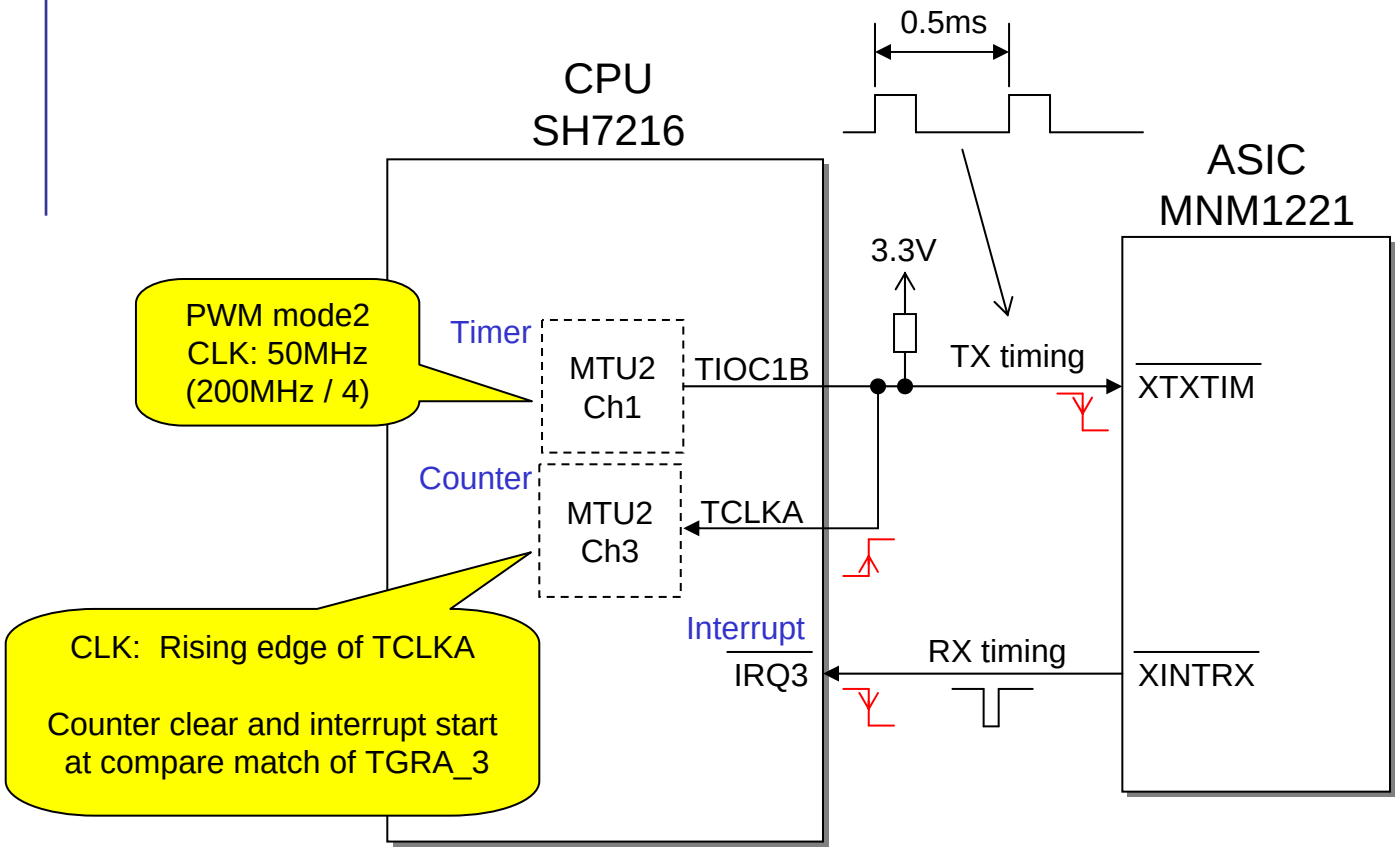
Revision	Date	Change Description
1	2012/10/30	Initial Release

Block Diagram



Master Mode

Timing Circuit for CPU-Timer



- MTU2-Ch1 generates TX timing signal. For 0.5ms, **TGRA_1 = 24999(0x61A7)@50MHz**
- MTU2-Ch3 divides this signal, and generates the start signal for NC calculating interrupt. For 1ms, **TGRA_3 = 1**
- IRQ3 by XINTRX of MNM1221 causes RX interrupt.

Communication Period Setting

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11.7.3 Caution on Period Setting

When counter clearing on compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula:

- Channel 0 to 4

$$f = \frac{P\phi}{(N + 1)}$$

- Channel 5

$$f = \frac{P\phi}{N}$$

Where f: Counter frequency
Pϕ: Peripheral clock operating frequency
N: TGR set value

50MHz

N = (50MHz / f) - 1

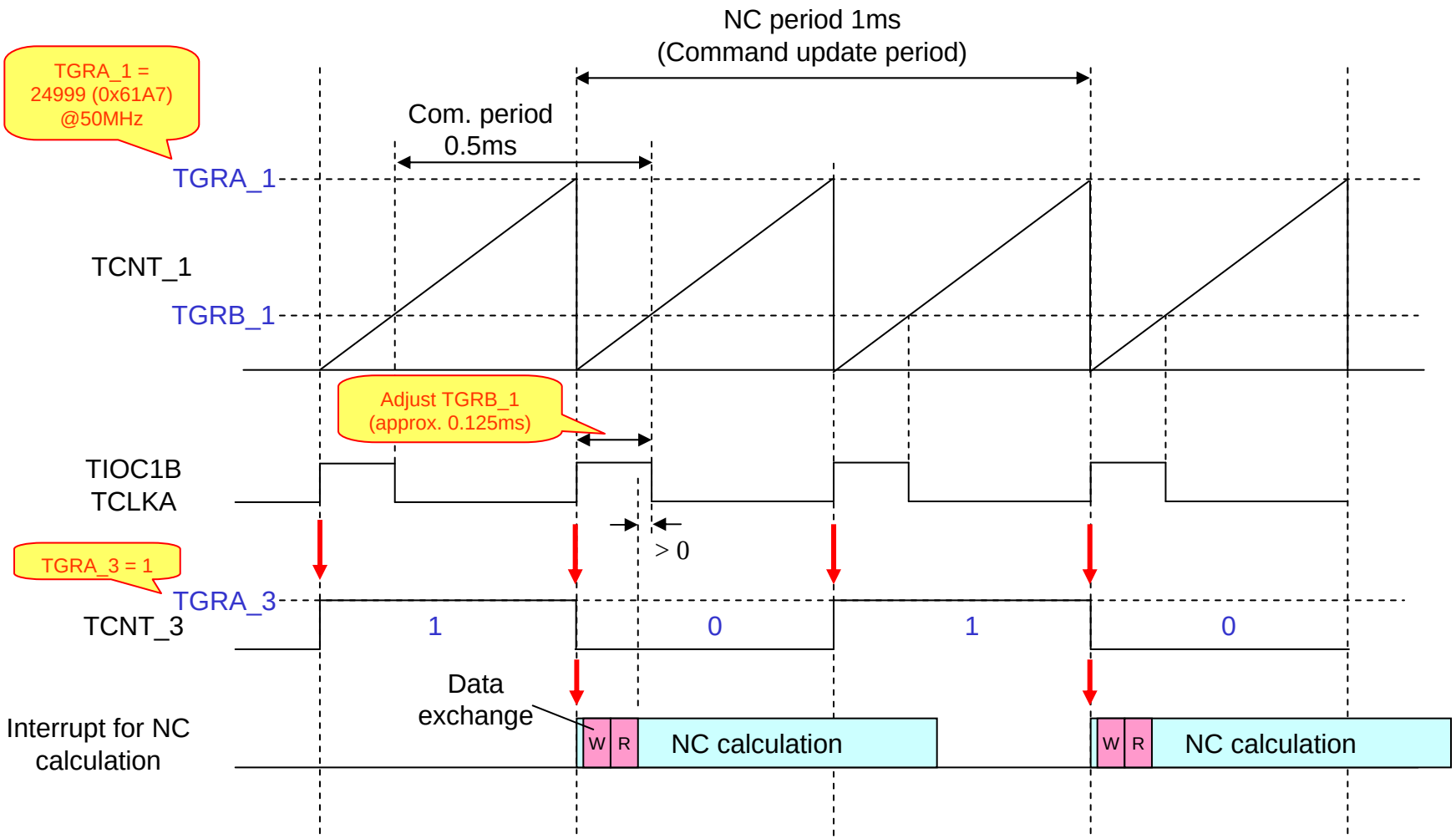
Com. Period	TGRA_1 setting value
1.000ms (1/1kHz)	49999 (0xC34F)
0.500ms (1/2kHz)	24999 (0x61A7)
0.1667ms (1/6kHz)	8332 (0x208C)
0.0833ms (1/12kHz)	4166 (0x1046)

Multiplex Interrupt Setting

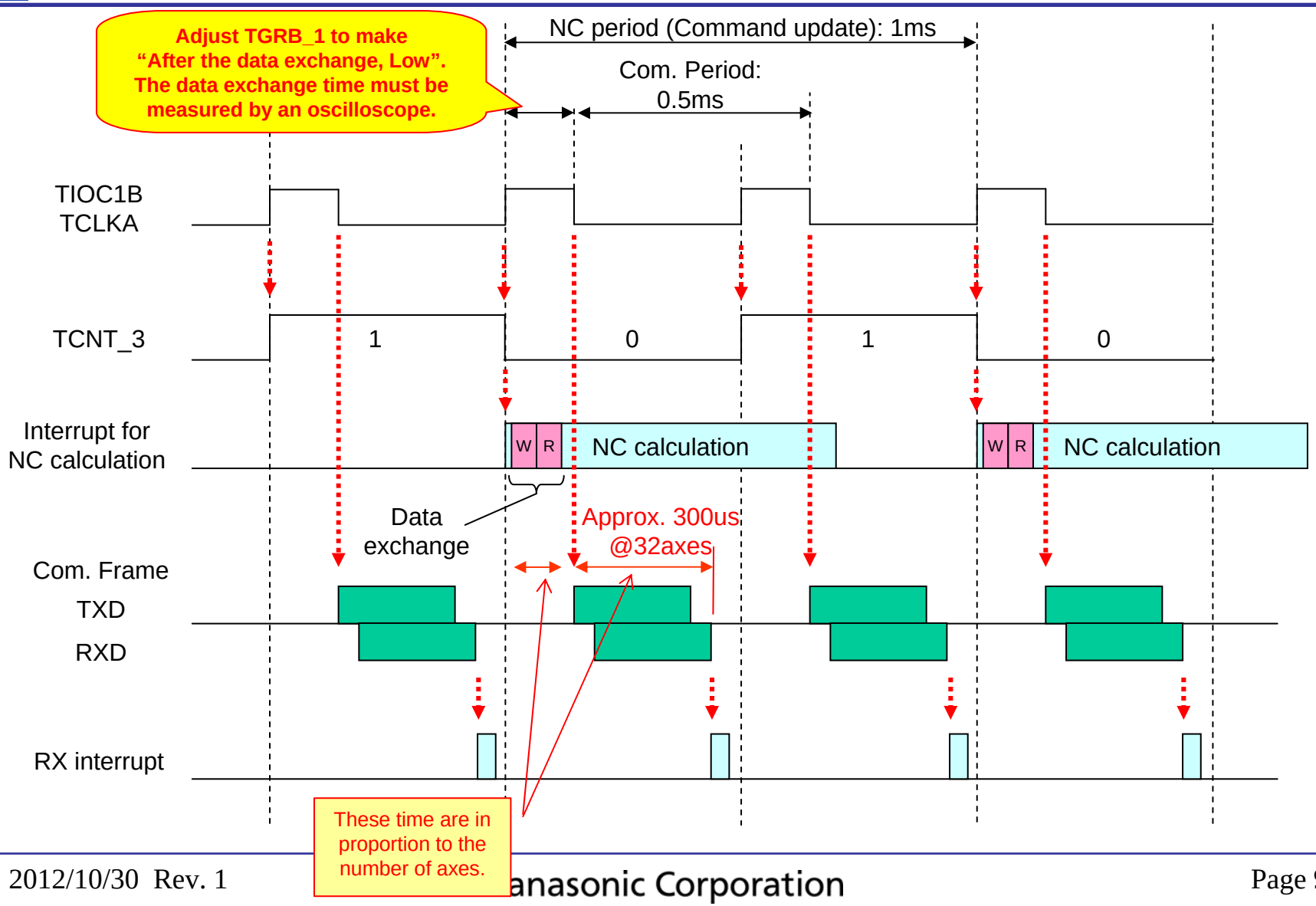
Source	Trigger	Priority	Period Example	Operation
TGIA_3	Compare match of MTU2 Ch3	-	1ms	- Communication data exchange - NC calculation
/IRQ3	RX complete	Higher than TGIA_3	0.5ms	- Communication status check - RX memory bank switch

Note:
If it is required that command update period is the same as communication period 0.5ms, TGIA_1 should be used instead of TGIA_3. In this case, an interrupt occurs by ch1 of MTU2 compare match.

Timing Chart 1



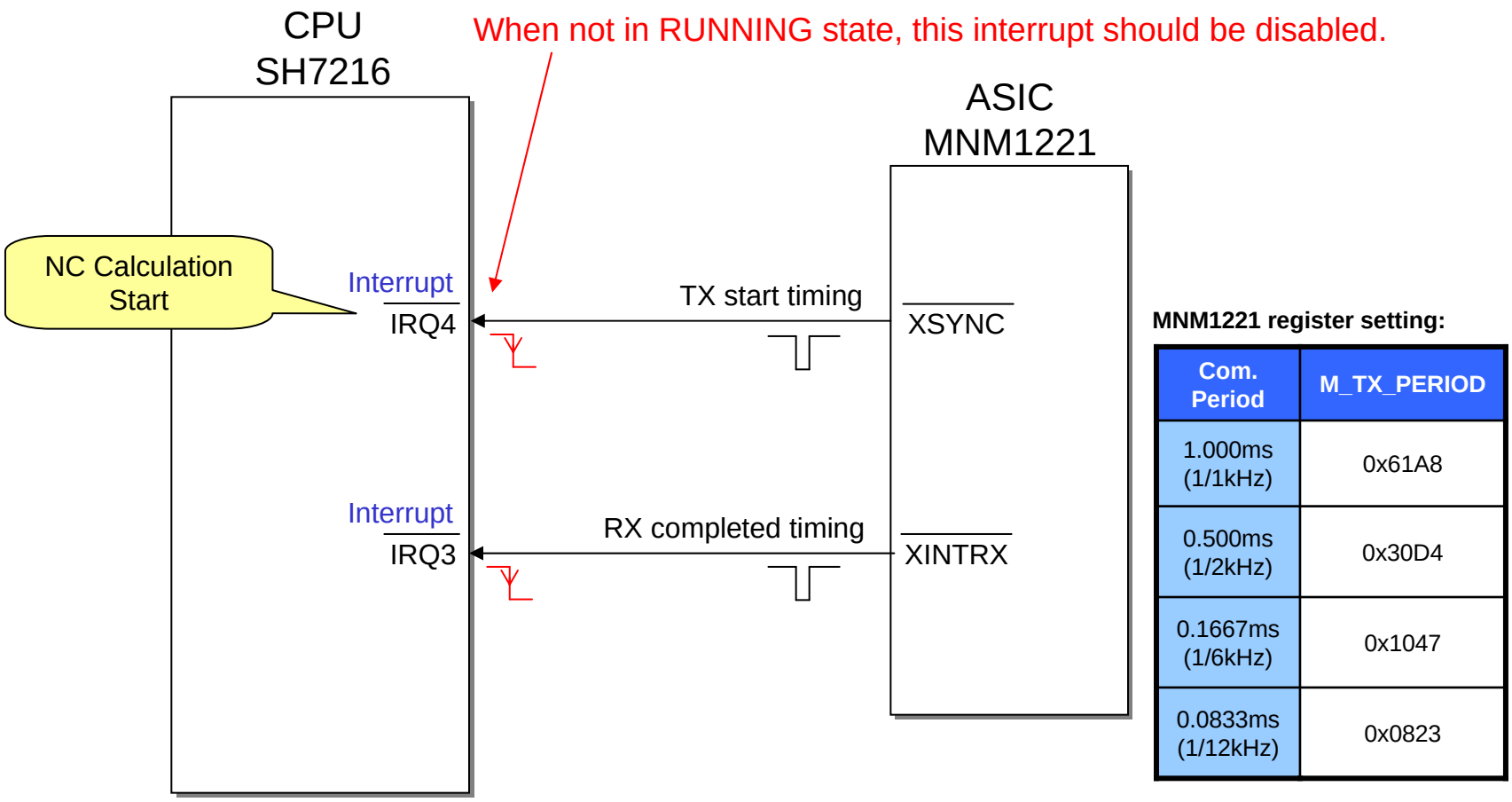
Timing Chart 2



Register Setting for MTU2

Register	Setting Value	Description
TCR_1	0x20	50MHz, Rising edge, TGRA compare clear
TCR_3	0x26	TCLKA, Rising edge, TGRA compare clear
TMDR_1	0x03	PWM mode2
TMDR_3	0x00	Normal mode
TIOR_1	0x52	0 output with TGRB_1, 1 output with TGRA_1
TIORH_3	0x00	
TIORL_3	0x00	
TIER_1	0x00	
TIER_3	0x01	TGIA_3 enable
TBTM_3	0x00	
TICCR_1	0x00	
TICCR_3	0x00	
TGRA_1	0x61A7	0.5ms
TGRB_1	0x186A	0.125ms (Adjust by test)
TGRA_3	0x0001	1ms
TSTR	0x42	Start ch1 and 3

Timing Circuit for MNM1221-Timer



MNM1221 register setting:

Com. Period	M_TX_PERIOD
1.000ms (1/1kHz)	0x61A8
0.500ms (1/2kHz)	0x30D4
0.1667ms (1/6kHz)	0x1047
0.0833ms (1/12kHz)	0x0823

Note: CPU-Timer based system is more recommended than this MNM1221-Timer.

Period Setting for A5N

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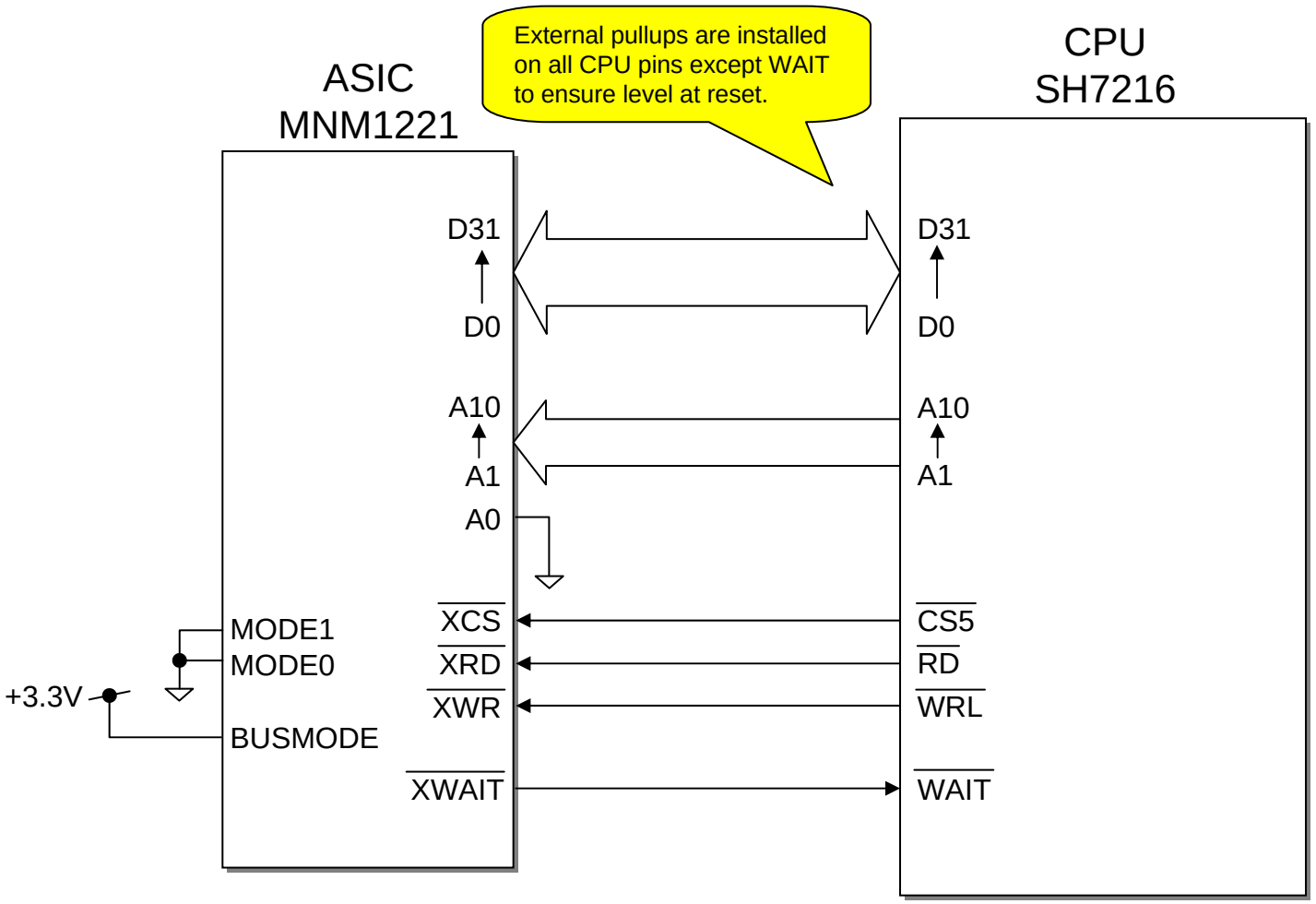
The period setting must be the same between master and slave.
For servo drive A5N, the setting is as follows:

Command Update Period	Com. Period	Setting	
		Pr7.20	Pr7.21
1.000ms	1.000ms	6	1
1.000ms	0.500ms	3	2
0.500ms	0.500ms	3	1
0.166ms	0.166ms	1	1
0.166ms	0.083ms	0	2

	Name	Range	Description
Pr7.20	Communication Period	0 to 12	0: 0.083ms 1: 0.166ms 3: 0.5ms 6: 1.0ms Else: Do not set. (Reserved)
Pr7.21	Ratio of Command Update Period	1 to 2	Command Update / Communication Period 1: 1 2: 2 (Com.=0.5ms case only) } Select

Bus Connection



Note: A1 connection is for 16bit bus access in slave mode.

Memory Map

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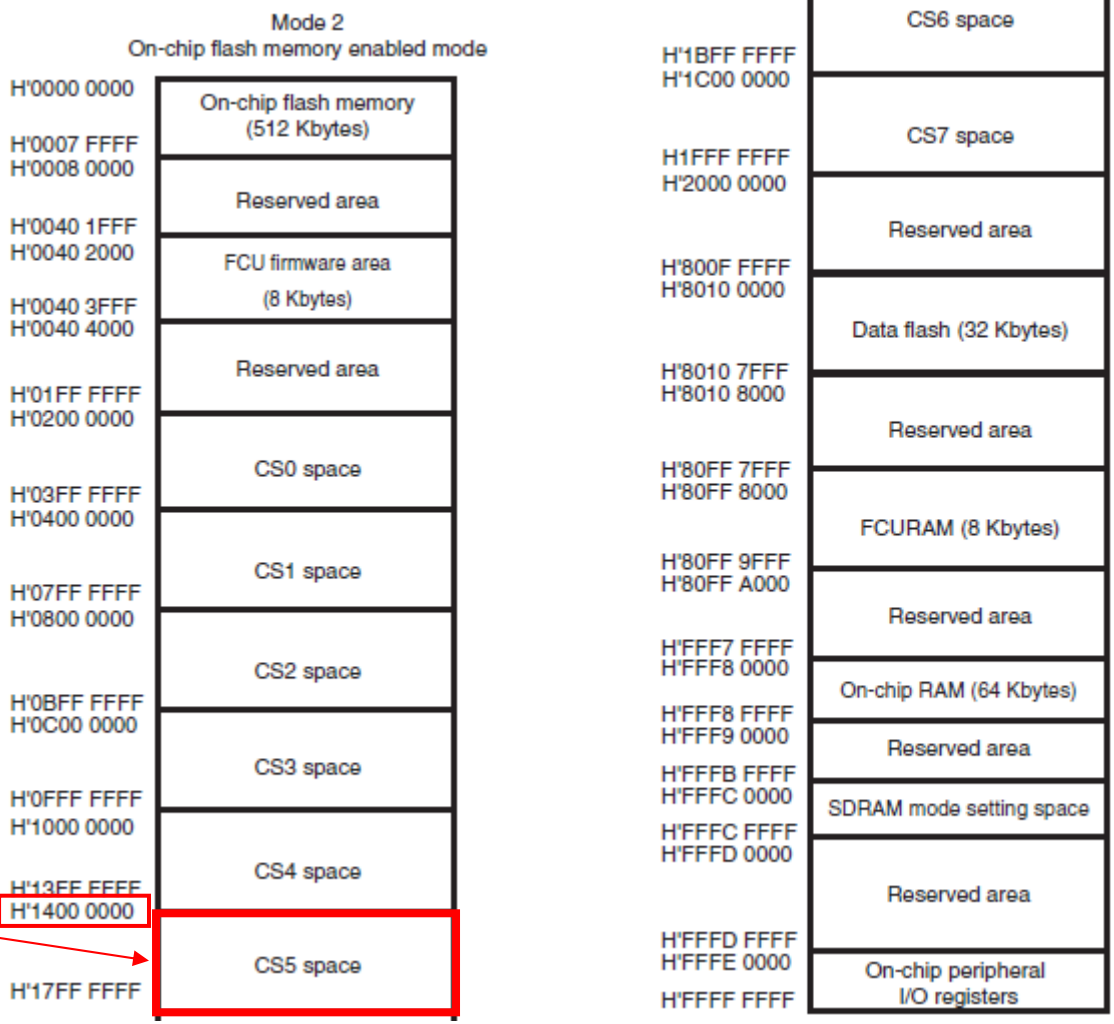
This map is for R5F72165BDFP (Flash 512K, RAM 64K)



MNM1221

In R5F72167BDFP, Flash 1M RAM 128K.

Modifying Example Code

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mnm1221_m.h

```
/*** IMPORTANT!!! ***/
/* You must modify the following definition according to your system. */
/*------------------------------------------------------------------------*/
/* Definition depend on your system                                       */
/*------------------------------------------------------------------------*/
/* Located Address of MNM1221 */
#define ADDR_MNM1221        0x08000000      /* unit: byte address */
                            0x14000000

/* Data Bus Width to access to MNM1221 */
#define MASTER_16BIT_ACCESS
/* If NOT 16bits BUT 32bits, change this definition to comments or delete it. */
/*------------------------------------------------------------------------*/
```

Modify this address value in order to suit to the located address of MNM1221.

Delete this line because of 32bit bus.

Register Setting for Bus

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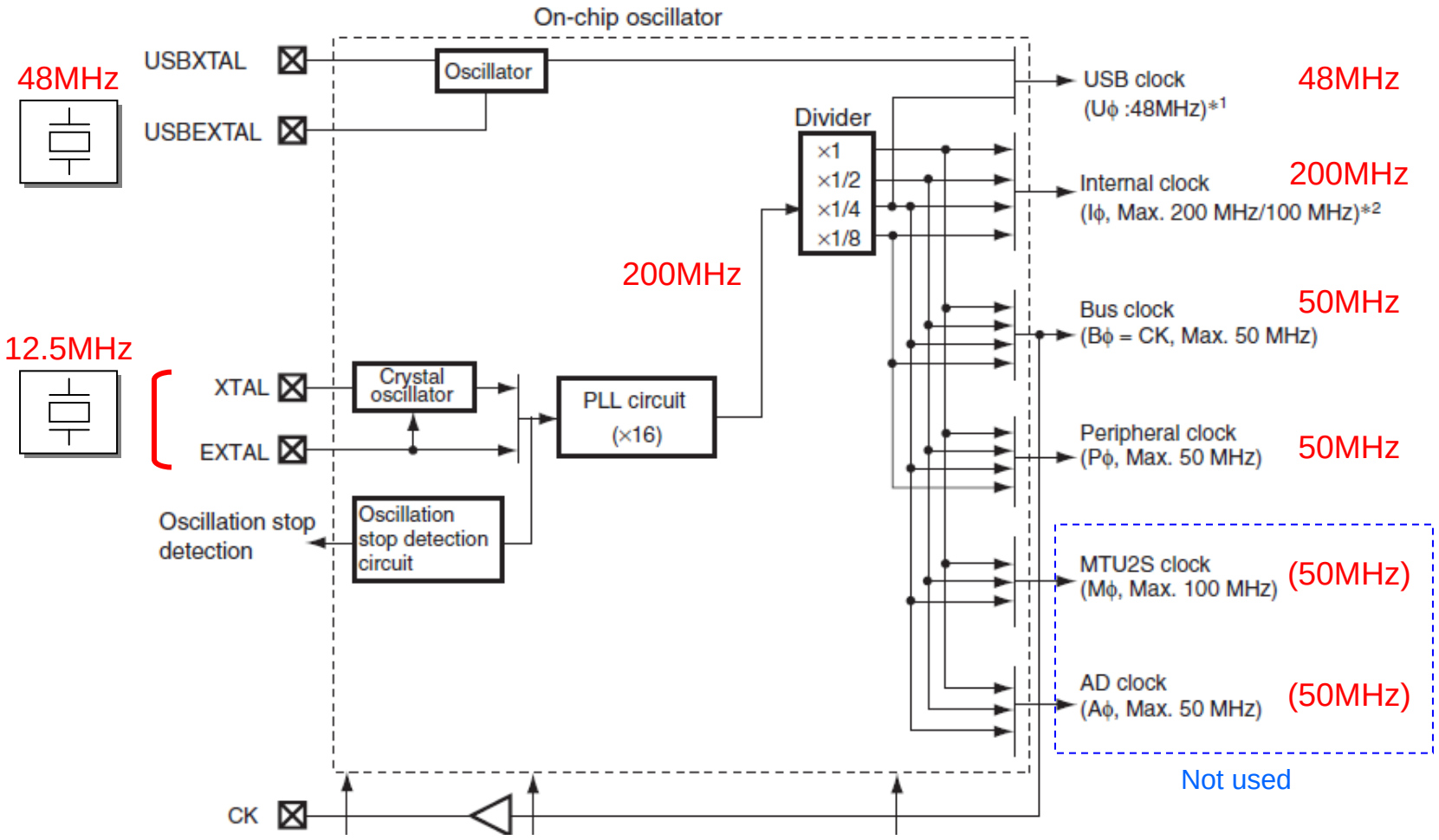
CS5 space:

Register	Setting Value
CS5BCR	0x24920E00
CS5WCR	0x00070300

- 2-idle cycle
- 32-bit bus width
- 6-wait cycle in R/W access
- External wait enable for Read access

Note: If 16-bit bus in slave mode, CS5BCR = 0x24920C00.

Clock

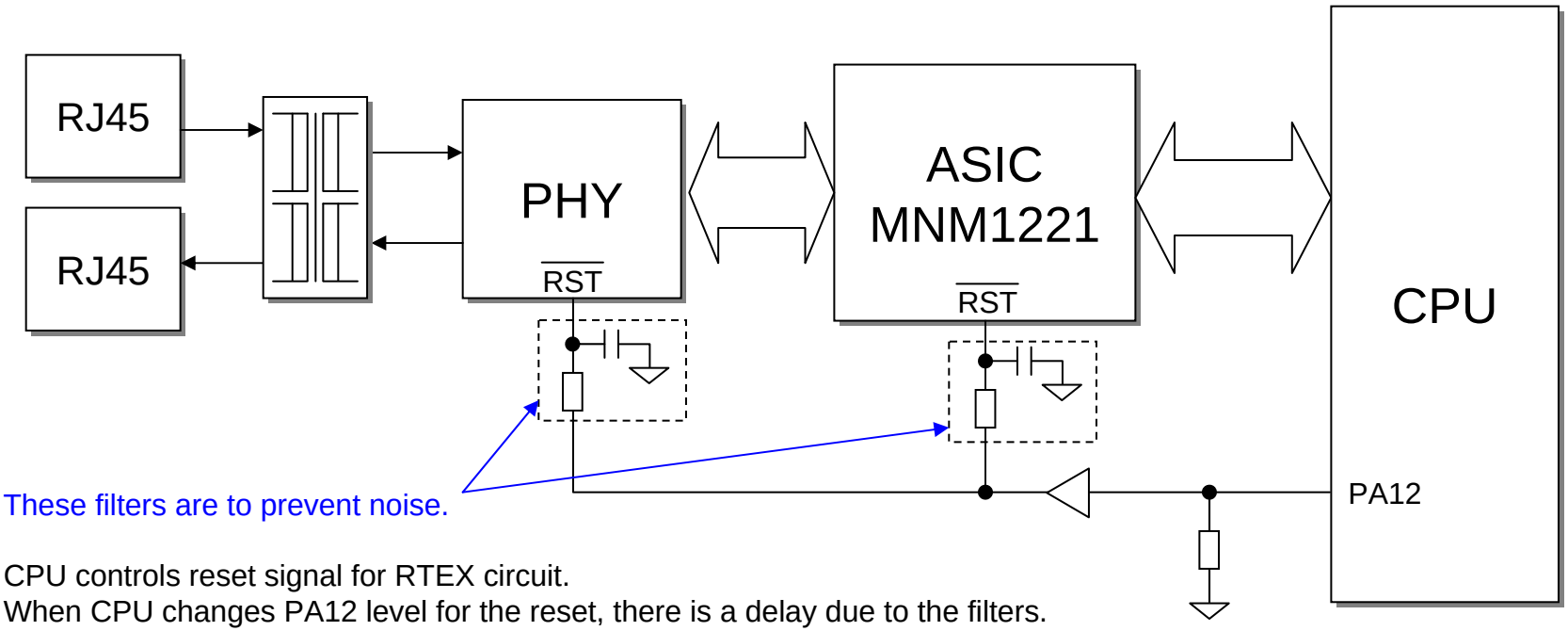

On-chip oscillator
48MHz
USBXTAL
USBEXTAL
Oscillator
Divider
×1
×1/2
×1/4
×1/8
USB clock
(Uϕ :48MHz)*1
48MHz
Internal clock
(Iϕ, Max. 200 MHz/100 MHz)*2
200MHz
200MHz
12.5MHz
XTAL
EXTAL
Crystal oscillator
PLL circuit
(×16)
Bus clock
(Bϕ = CK, Max. 50 MHz)
50MHz
Peripheral clock
(Pϕ, Max. 50 MHz)
50MHz
Oscillation stop detection
Oscillation stop detection circuit
MTU2S clock
(Mϕ, Max. 100 MHz)
(50MHz)
AD clock
(Aϕ, Max. 50 MHz)
(50MHz)
Not used
CK

Register Setting for Clock

Register	Setting Value
FRQCR	0x0303
MCLKCR	0x43
ACLKCR	0x43
OSCCR	0x00
STBCR3	0x56
STBCR4	0xE7
STBCR5	0xBF
STBCR6	0x9F

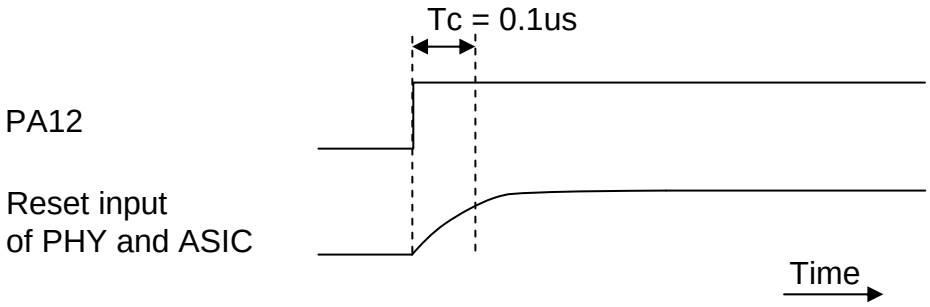
- MTU2, IIC and flash enable
- SCIF enable
- SCI1 enable
- USB OSC enable

Reset for RTEX Circuit



These filters are to prevent noise.

CPU controls reset signal for RTEX circuit.
When CPU changes PA12 level for the reset, there is a delay due to the filters.
Therefore CPU cannot access the MNM1221 for a moment after releasing the reset.



Although PA12 is Hi-Z at CPU reset, this resistor ensures low level.
If watchdog timer overflows, RTEX circuit should be reset for safety.
This reset causes communication timeout, and all servos will stop with timeout alarm.

Register Setting for WDT

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After setting the followings, set WTCNT to 0x00 periodically.

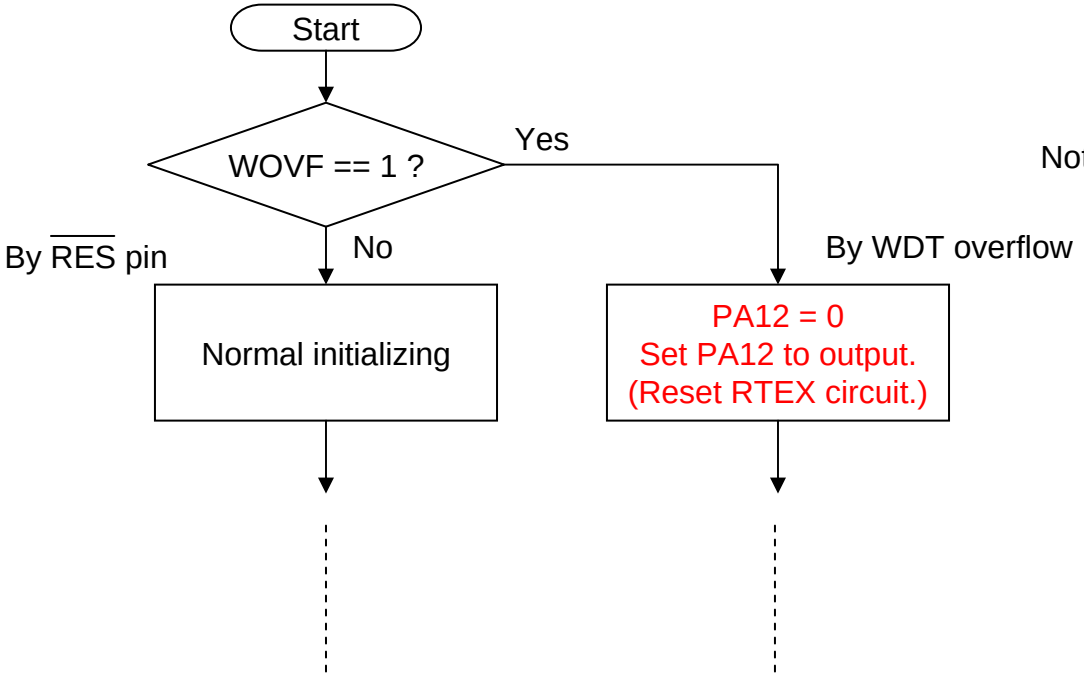
Register	Setting Value
WTCNT	0x00
WTCSR	0x7D
WRCSR	0x5F

- WDT counter clear
- WDT enable
- WDT overflow period is 5.2ms as an example.
- If WDT overflows, do power-on-reset.

Note:
It is not normal way to write these registers.
For details, see SH7216 user's manual for hardware.

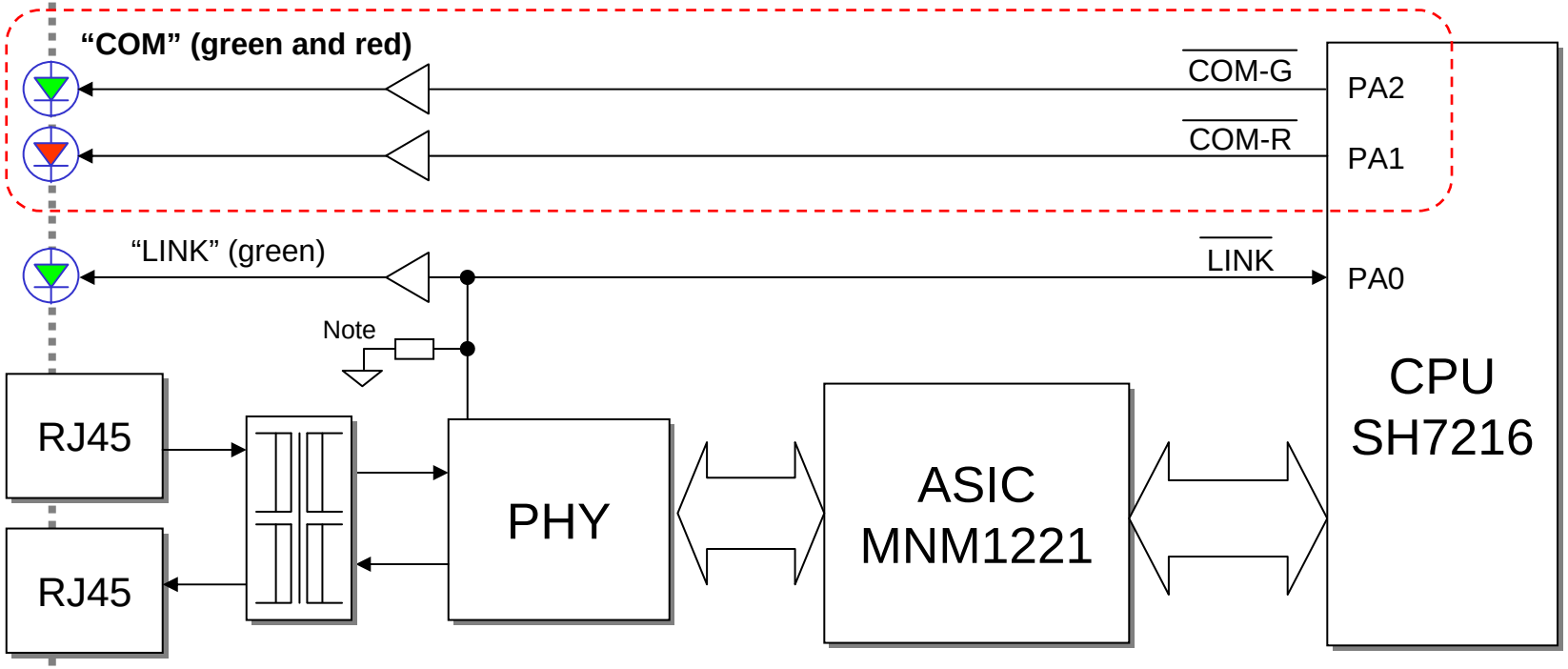
Distinguishing WDT Overflow

After releasing power-on-reset, put a distinguishing as follows.



Note: WOVF is on WRCSR register.

Status LEDs for Communication



Note:
On PHY link pin, a pull-down is installed for pin configuration.
Regardless of actual link situation, this pull-down causes LINK active at reset.

“COM” LED Operation

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“COM” LED which has red and green lights should be operated as follows:

Normally

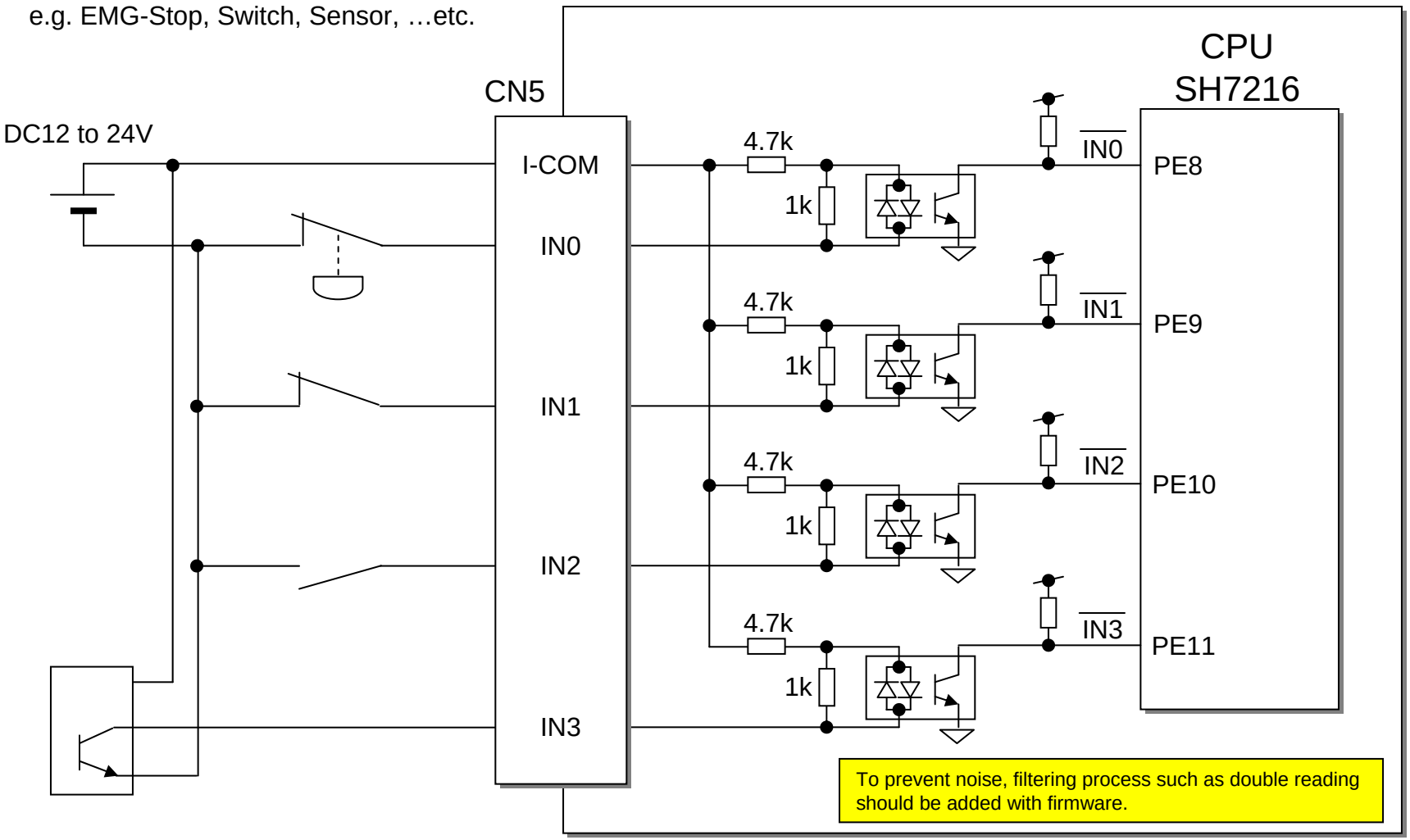
Return value of ctrl_mnm1221_m() in the example code	“COM” LED operation
PH_INIT	Disappearance
PH_WAITING	Flashing Green (0.5s ON, 0.5s OFF)
PH_PREPARE	
PH_START	
PH_RUNNING	Solid Green

Error detected

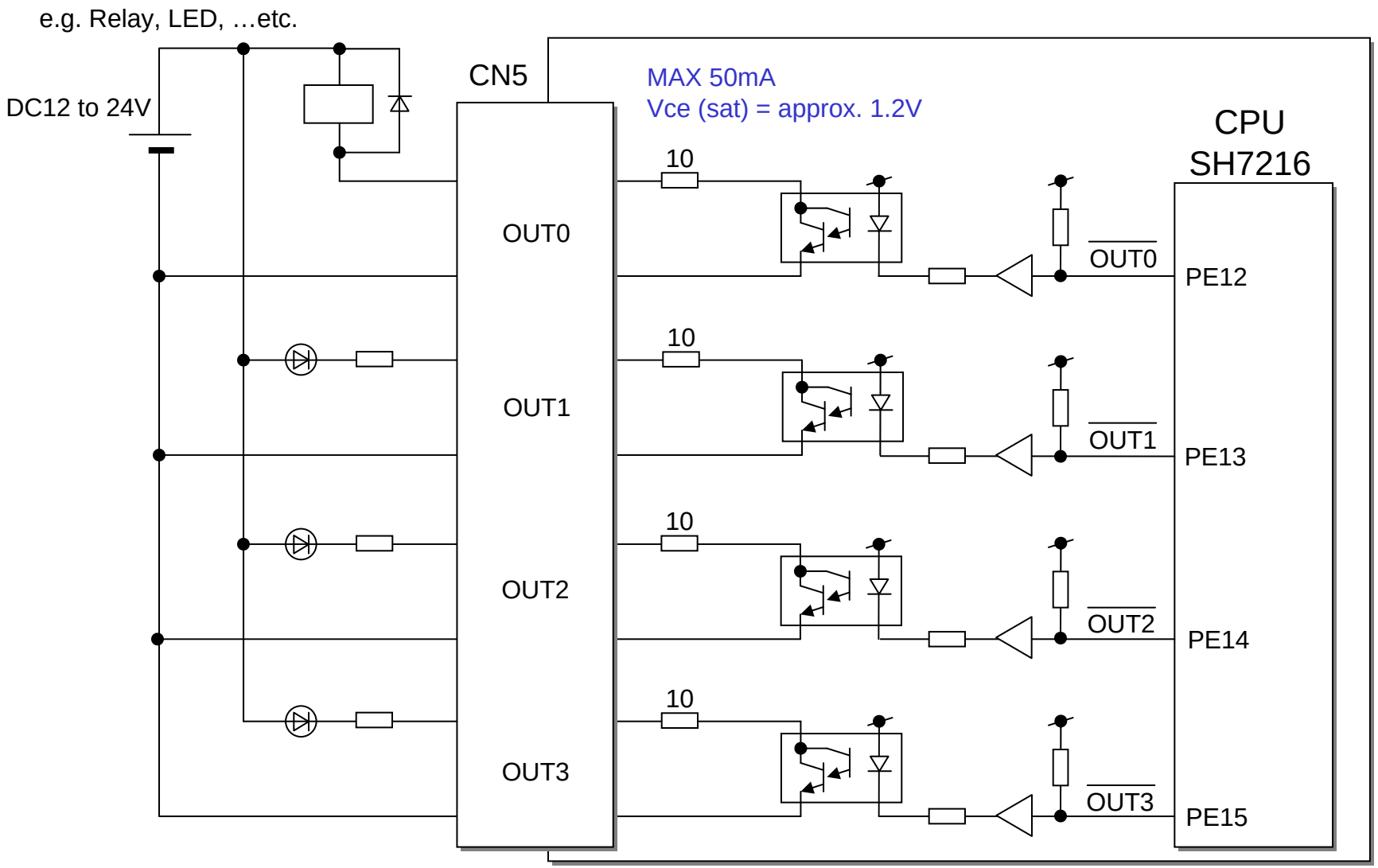
Contents of error	“COM” LED operation
Timeout in RUNNING state	Flashing Red (0.5s ON, 0.5s OFF)
Mismatch of slave information (e.g. duplicate MAC-ID)	Solid Red

Notes:
- Solid Red means that a system reset is necessary to release the error.
- Either green or red must be lighted.

General Purpose Inputs



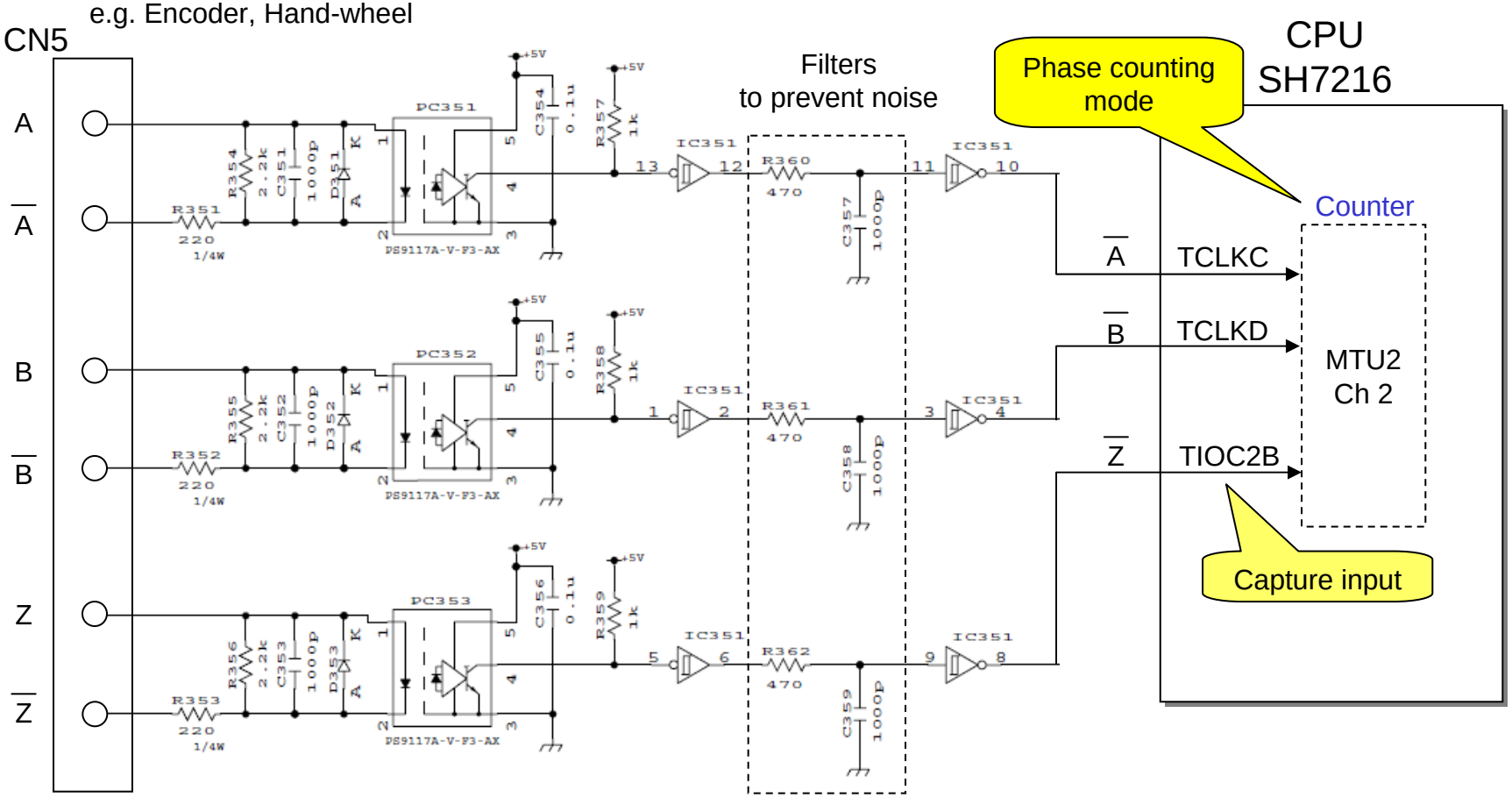
General Purpose Outputs



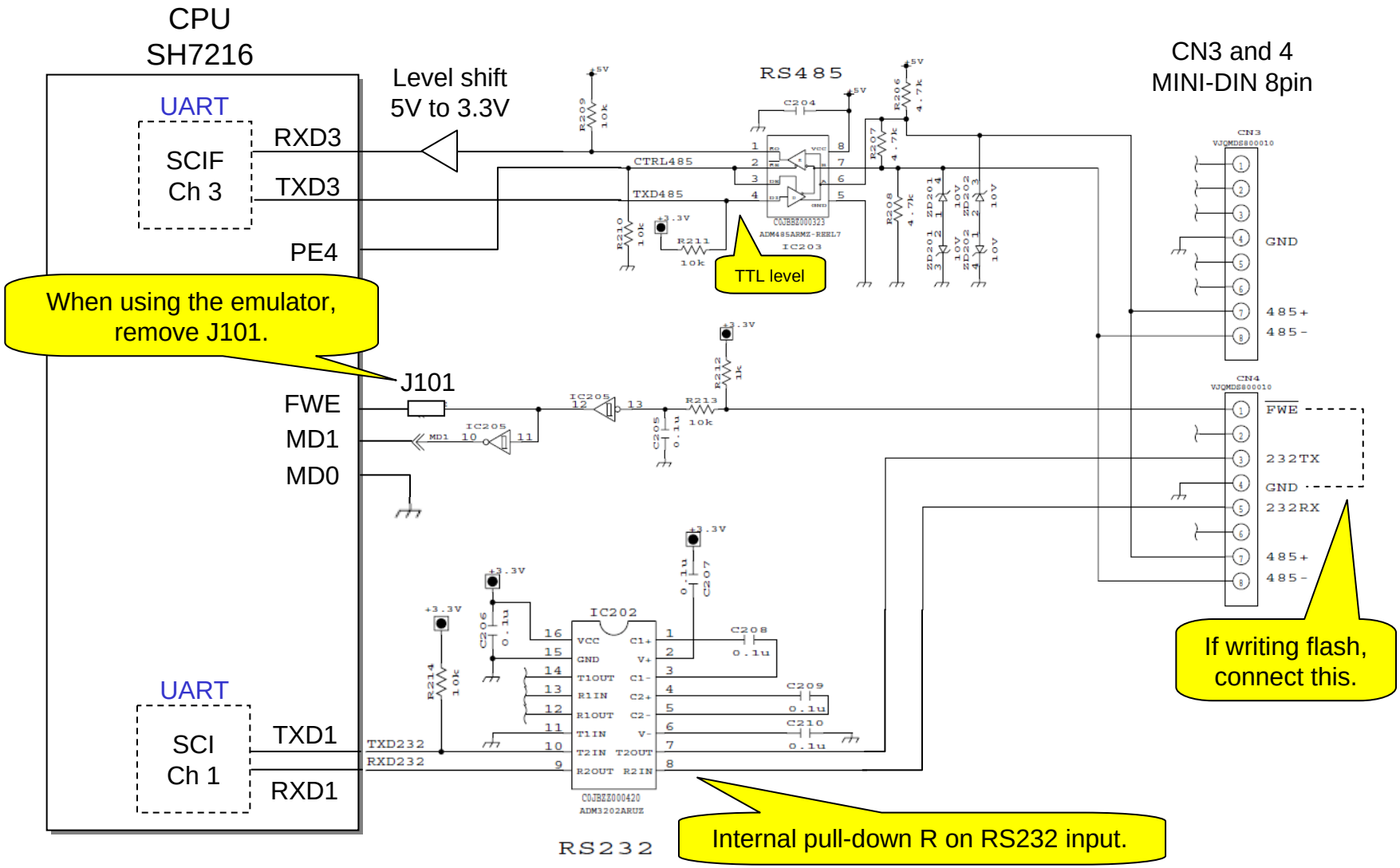
A/B/Z-Phase Inputs

For RS422 line driver signal

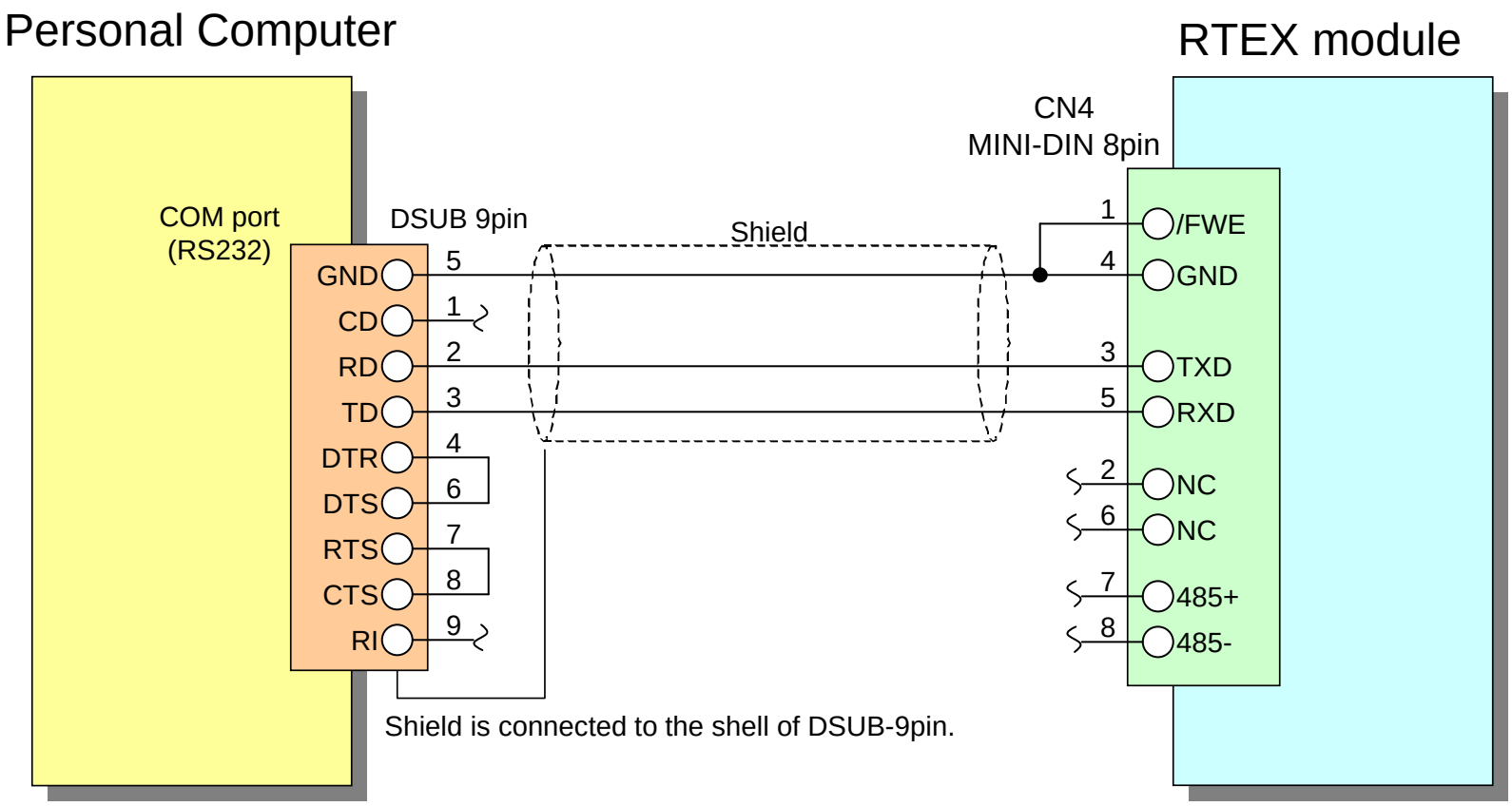
e.g. Encoder, Hand-wheel



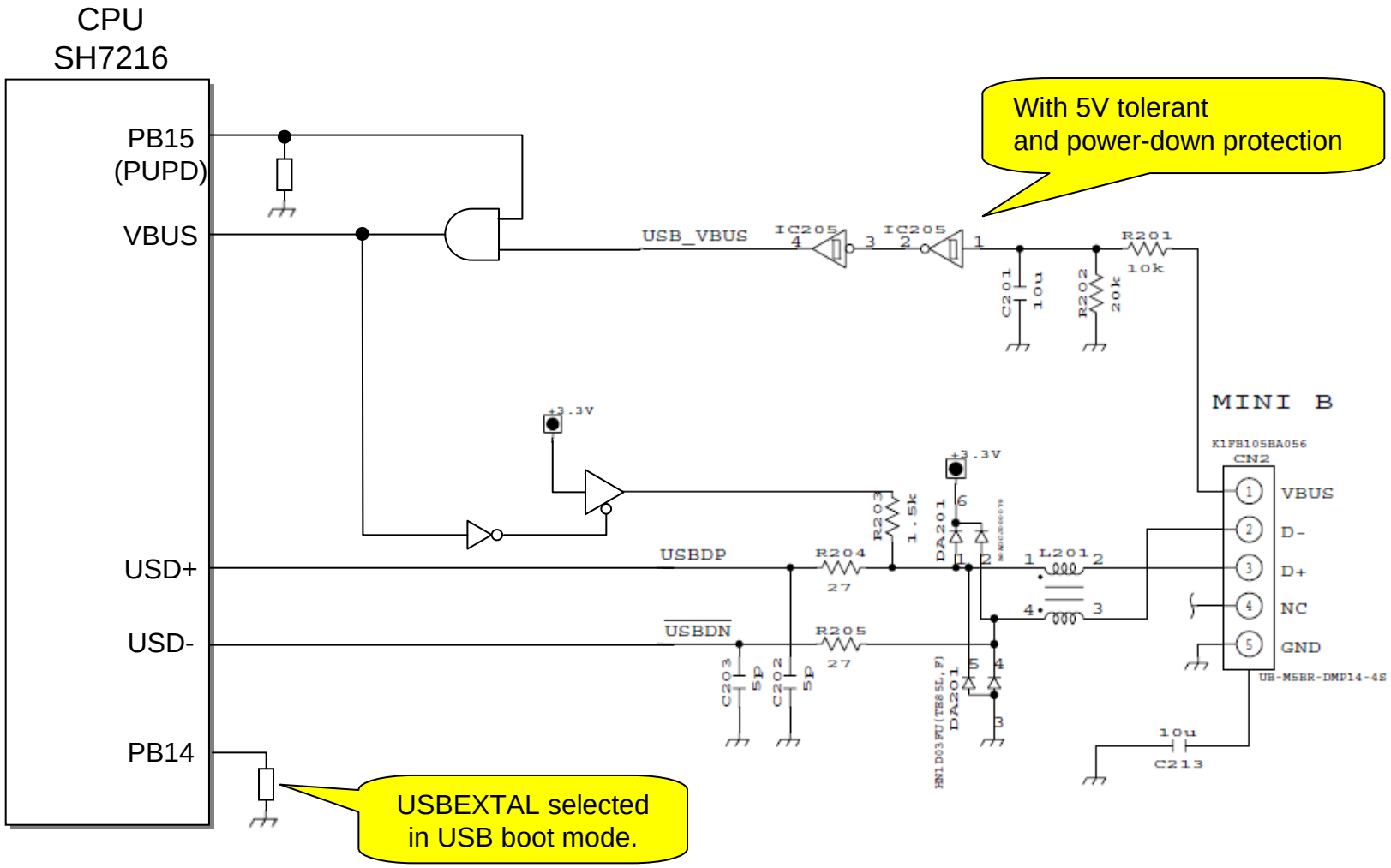
RS232/485 Interface



Cable Wiring for Flash-writing

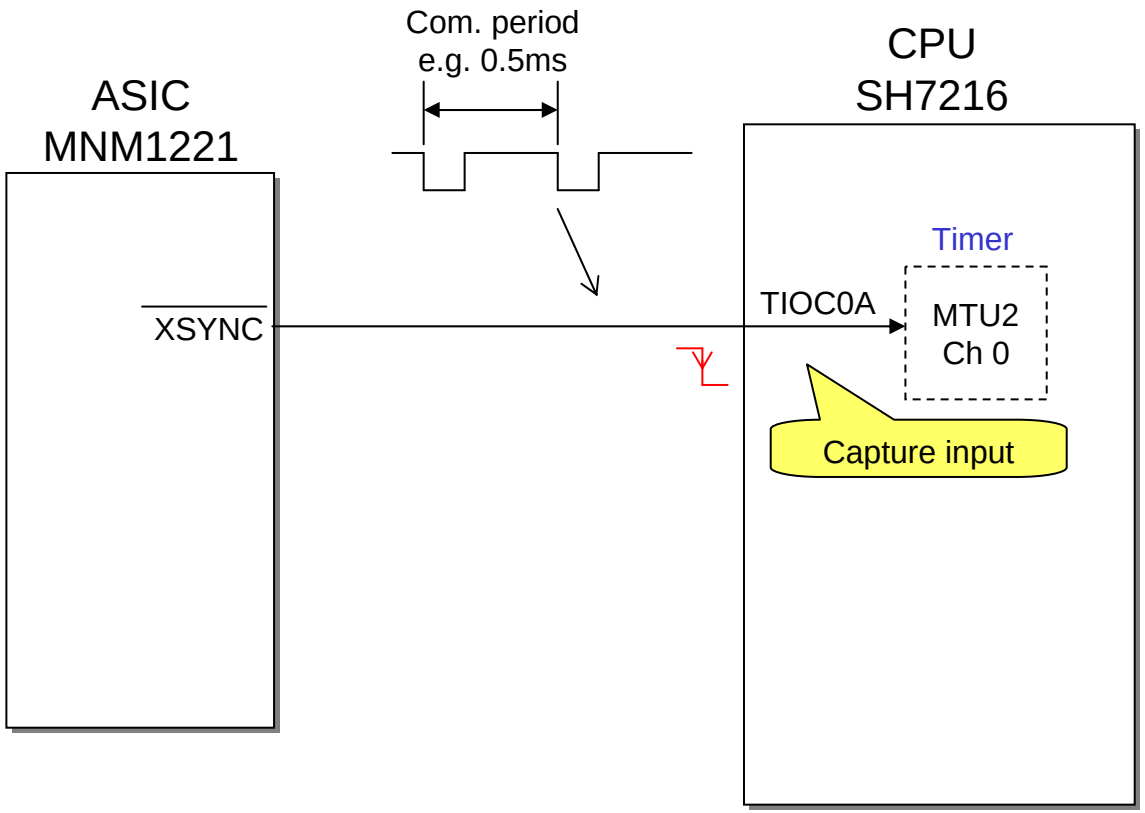


USB Interface



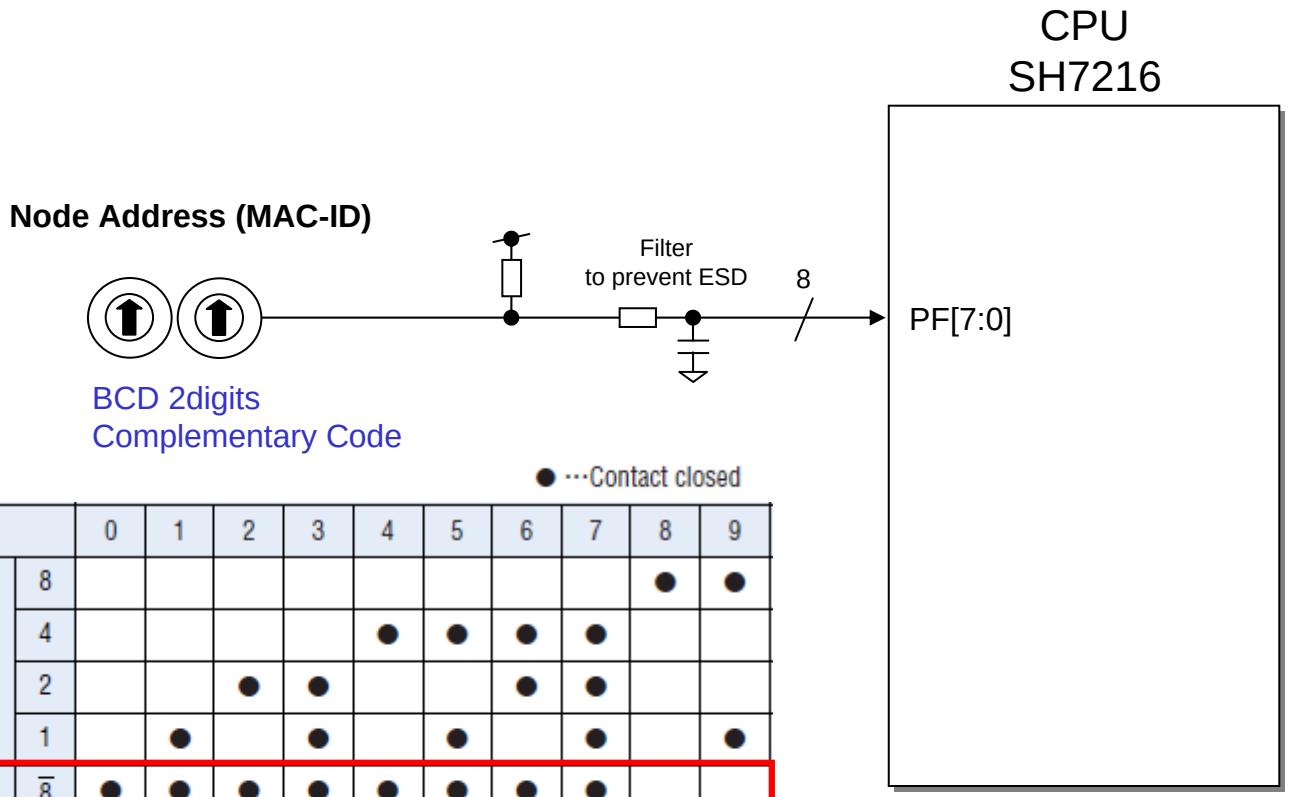
Slave Mode

Timing Circuit for Slave



- Connect XSYNC to a capture input of a timer built in the CPU.
- At the falling edge, the timer is cleared and the interrupt occurs.

RSW for Node Address



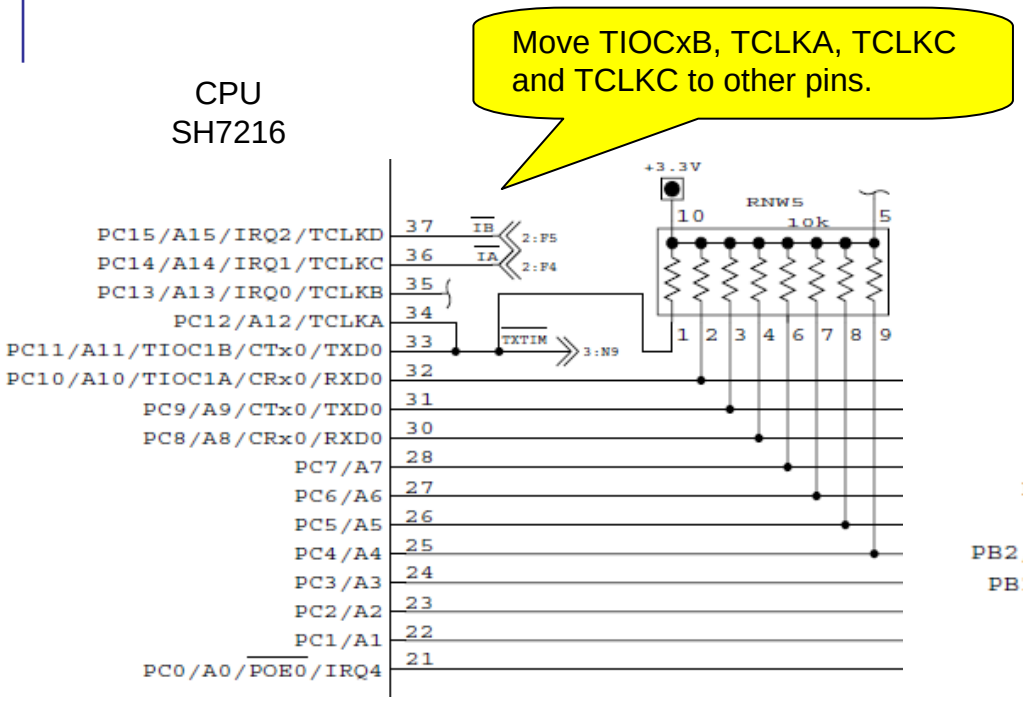
● ···Contact closed

Position			0	1	2	3	4	5	6	7	8	9
Code	Real code	8									●	●
		4					●	●	●	●		
		2			●	●			●	●		
		1		●		●		●		●		●
	Complementary code	$\overline{8}$	●	●	●	●	●	●	●	●		
		$\overline{4}$	●	●	●	●					●	●
		$\overline{2}$	●	●			●	●			●	●
		$\overline{1}$	●		●		●		●		●	

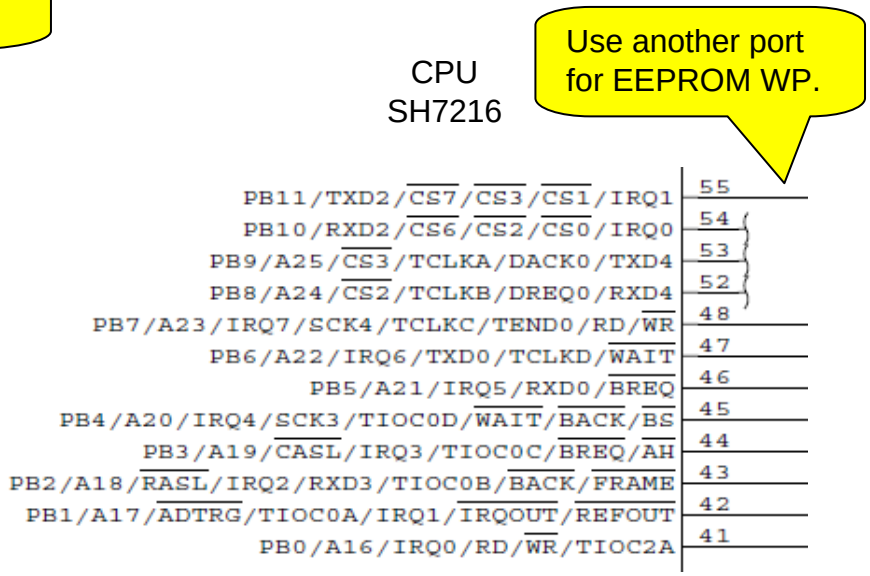
Modification

Adding External Memory

If additional memory is required, modify as follows.



Replace these pins as A[15:0].



Replace these pins as A[25:16] and CS.

Test LED Modification

If 2-digit 7-segment LED is required, modify as follows.